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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/763,858	01/21/2004	Haruki Ito	9319I-000651	9075

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EXAMINER	
LEE, CHEUNG	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 02/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/763,858	ITO, HARUKI	
	Examiner	Art Unit	
	Cheung Lee	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 32-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 32-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2-6-06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILD ACTION

Notice to Applicant

1. Applicant's Amendment and Response to the Office Action mailed on December 7, 2005 has been entered and made of record.

Response to Amendment

2. In view of Applicant's Amendment to the specification, the objection to the specification has been withdrawn.

3. In view of Applicant's Amendments and arguments filed on December 7, 2005, the rejections of claims 1-9 under 35 U.S.C. 103(a), as stated in the above indicated Office Action, have been withdrawn. Applicant's arguments have been rendered moot in view of the new ground of rejection given below.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-9 and 32-34 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. With respect to claim 1, it is not clear if "ones of the plurality of recesses" means two recesses, three recesses, or more recesses. The examiner cannot determine in how many recesses interior the interconnecting line needs to contact within.

Claims 2-9 and 32-34 depend from claim 1, so they are rejected for the same reason.

6. With respect to claim 2, it is not clear if "a transparent-and-opaque pattern" is defining the same pattern with "a pattern". The examiner cannot determine which pattern prevents the photosensitive resin precursor from being completely resolved.

Claims 3-4 depend from claim 2, so they are rejected for the same reason.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 5-7 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuchi (US Pub. 2002/0005568) in view of Yoda (JP Pat. 2001-144217).

8. With respect to claim 1, referring to figures 1-14B, Kikuchi discloses a method of manufacturing a semiconductor device (page 2, paragraph 30) comprising: forming a resin layer 140 on a semiconductor substrate 110, the substrate is obviously be a semiconductor substrate since Kikuchi discloses the semiconductor device, in which a plurality of integrated circuits are formed (page 2, paragraph 32; page 5, paragraph 91); forming a recess (142, 901) in a surface of the resin layer making the resin layer surface uneven; forming an interconnecting line on the resin layer, the interconnecting line 303 contacting the surface of the resin layer within an interior of the recess along which the

interconnecting line passes (see fig. 10D); and cutting the semiconductor substrate into a plurality of semiconductor chips (page 2, paragraph 37; page 6, paragraph 100). According to Kikuchi, the protective layer 130 and resin layer 140 have total thickness of 2 μm (page 2, paragraphs 39-40), so the recesses depth in figure10B is at least 1μm. However, Kikuchi does not disclose expressly forming a plurality of recesses wherein each of the plurality of recesses is formed to have an opening width less than a thickness of the interconnecting line. Kikuchi discloses a recess improving the adhesion between the interlayer film and the metallic thin film (page 2, paragraph 40). Therefore, the examiner takes the position that the width of the recess have to be chosen to fulfill this objective while not degrading the characteristics of the insulating layer (resin and protective layers) and vary with the requirements of a specific application.

Referring to figures 1-10, Yoda discloses a plurality of recesses 24 forming in a surface of a resin layer 20 (see fig. 1A), and an interconnecting line 30, which contacts the surface of the resin layer within an interior of the recesses (see fig. 4A).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to form a plurality of recesses instead of one single recess, as taught by Yoda.

The motivation for doing so would have been to ease a stress applied to the connection for the electric connection with the exterior and easily form a resin layer in longitudinal direction (Yoda, paragraph 5).

9. With respect to claim 5, Kikuchi in view of Yoda discloses wherein roughening the surface of the resin layer including inner surfaces (Kikuchi, page 4, paragraphs 69)

of the recess after forming the recess and before forming the interconnecting line (Yoda, paragraph 48).

10. With respect to claim 6, Kikuchi in view of Yoda discloses wherein forming a second resin layer (Yoda, 110) on the resin layer (Yoda, 20) to cover at least a part of the interconnecting line (see Yoda's fig. 7), after forming the interconnecting line and before cutting the semiconductor substrate. According Yoda's figure 7, the second resin layer is formed after forming the interconnecting line and before cutting the semiconductor substrate.

11. With respect to claim 7, Kikuchi in view of Yoda discloses wherein forming recesses (Yoda, 114) and projections (see Yoda's fig. 7) on a surface of the second resin layer.

12. With respect to claim 33, Kikuchi in view of Yoda discloses wherein the recesses are disposed in an isolated manner in plan view (see Yoda's figs. 6 and 8).

13. Claims 2-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuchi in view of Yoda, as applied above, and further in view of Wolf et al. ("Silicon Processing for the VLSI Era", Vol. 1, Ch. 12, page 407-409; hereinafter "Wolf").

14. With respect to claim 2, Kikuchi in view of Yoda discloses wherein the resin layer is formed of a photosensitive resin precursor (Yoda, paragraph 47), in the step of forming the recesses, photolithography using a mask is applied (Yoda, paragraph 47), carrying out light irradiation (Yoda, paragraphs 45 and 47), but Kikuchi in view of Yoda does not disclose expressly a transparent-and-opaque pattern mask; a pattern which

prevents the photosensitive resin precursor from being completely resolved, and which prevents the recesses from penetrating an entire thickness of the resin layer. Since Yoda discloses the patterned resin layer with recesses as shown in figure 1A, so a pattern to form this structure with light irradiation obviously prevents the photosensitive resin precursor from being completely resolved, and also prevents the recesses from penetrating an entire thickness of the resin layer.

Wolf discloses lithography process using a mask containing clear and opaque features for carrying out light irradiation (page 407, bottom portion and fig. 1).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use a mask to perform the lithography as conventionally done to obtain desired patterns.

15. With respect to claims 3 and 4, the combine teaching of Kikuchi, Yoda and Wolf discloses wherein the photosensitive resin precursor is a negative type including an insoluble light-sensitive portion (Wolf, page 407 and fig. 1), but the combine teaching of Kikuchi, Yoda and Wolf does not disclose expressly wherein the transparent-and-opaque pattern includes [Claim 3] an opaque portion having a width less than or equal to the thickness of the interconnecting line, and wherein [Claim 4] the width of the opaque portion is less than or equal to one-fourths of a thickness of the resin layer. The opaque portion is to form recesses, so recesses' dimensions reflect to the opaque portion's dimensions. The arguments concerning recesses' dimensions stated in claim 1 also apply.

16. Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuchi in view of Yoda, as applied above, and further in view of Ma (US Pat. 6713859).

17. With respect to claim 8, Kikuchi in view of Yoda does not disclose wherein forming a third resin layer on the second resin layer.

Referring to figures 3A-3O, Ma discloses a third resin layer (fig. 3O, item 374) on the second resin layer (fig. 3O, item 338).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use multiple resin layers, as taught by Ma.

The motivation for doing so would have been to achieve protection of the device against moisture encroachment and delamination, and against any cracking of the semiconductor element.

18. With respect to claim 9, the combine teaching of Kikuchi, Yoda and Ma discloses wherein forming recesses and projections on a surface of the third resin layer. Ma discloses forming recesses and projections (fig. 3I, items 342 and 344) on a surface of the second resin layer (fig 3I, item 338), and this process is repeated until a build-up layer is complete, as shown in figure 3O (col. 6, lines 55-67). So, it would have been obvious to have the steps of forming recesses and projections on the third resin layer surface when more wiring layers are required.

19. Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuchi in view of Yoda, as applied above, and further in view of Kida et al. (US Pat. 6313540; hereinafter "Kida").

Kikuchi in view of Yoda does not disclose expressly wherein the recesses form an interconnected lattice in plan view.

Referring to figures 7a-8, Kida discloses a plan view of arrangement of opening portions 21c of via-holes 21 and a pad 3, and an interconnected lattice shape is shown in figure 7c.

It would have been obvious that the dispositions of the recesses have to be chosen in various forms to fulfill the requirements of a specific application.

20. Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuchi in view of Yoda, as applied above, and further in view of Kuwabara et al. (US Pub. 2002/0008320; hereinafter "Kuwabara").

Kikuchi in view of Yoda does not disclose expressly wherein the recesses include a group of concentric ring-shaped recesses in plan view.

Kuwabara discloses a plan view of a semiconductor device, concentric ring-shaped, as shown in figure 17 on sheet 11 (page 8, paragraph 167).

It would have been obvious that the dispositions of the recesses have to be chosen in various forms to fulfill the requirements of a specific application.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cheung Lee whose telephone number is 571-272-5977. The examiner can normally be reached on Monday through Friday from 8:30AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cheung Lee

February 8, 2006

HA NGUYEN
PRIMARY EXAMINER